

The Programmable Logic Device Handbook

• Written by Von L. Burton • 480 pages • 452 illustrations • Hardcover with dust jacket
• \$49.95, Order No. 3140H • Published November 1989



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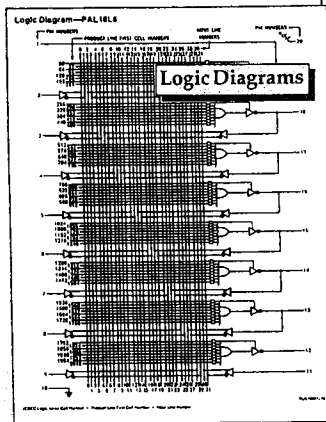
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PLD Architectures Require Scrutiny

Selecting an efficient PLD means matching the correct device architecture to your application. Therefore, you must know the strengths and weaknesses of each device. Trying to find the proper architecture for your application can be confusing.

The *Programmable Logic Device Handbook* cuts through the confusion. How many gates and flip-flops can you use? How many are available in a particular device? The handbook considers these factors in the overall device architecture so you can determine their usefulness for your application.



Logic Diagrams

Part Number	Part Type	Package	Pin Outcode	Pin	Inputs	I/O's	Regs	Macro Configs	Prog. Arrays	Product/Sum Terms	Prog Delay con(S)	Supply Current Icc(mA)	Current Z-Mode
153	Peel	Dip	8C/85	20	8	10	0	2	AND/OR	42/10	N/A	60mHz	no
173	Peel	Dip	8D/75	24	12	10	0	2	AND/OR	42/10	N/A	60mHz	no
180V8	Peel	Dip	8D/54	20	10	8	8	12	AND	74	15-25	70mHz	no
20CG10	Peel	Dip	8D/55	24	12	10	10	4	AND	90	15-20	70mHz	no
20CG10Z	Peel	Dip								92	15-20	45 + 1 0mHz	yes
22CV10	Peel	Dip								132	15-20	45 + 0.7mHz	no
22CV10Z	Peel	Dip								132	15-20	45 + 0.7mHz	yes
253	Peel	Dip								132	15-20	45 + 0.7mHz	yes
273	Peel	Dip								132	15-20	45 + 0.7mHz	yes

System Diagrams

Screens

INTEL PROGRAMMABLE LOGIC SOFTWARE II

- HELP
- IPLS
- INPUT FORMAT
- FILE NAME(S)
- MINIMIZATION
- INVERSION CONTROL
- ERROR FILE EXECUTE

ADD MINIMIZATION LEF-ANALYSIS X CONTROL
 INFO-LOC-BEGIN EXECUTION
 INFO-LOC-4 MACROFUNCTIONS RESOLVED IN X CONTROL
 INFO-LOC-SUM OF PRODUCTS (S.O.P.) LEF PRODUCED
 INFO-LOC-LEF REDUCED
 INFO-LOC-LEF ANALYZED
 INFO-LOC-RESOURCE DEMAND DETERMINED
 INFO-LOC-DESIGN FITTING COMPLETE
 INFO-LOC-JEDEC FILE OUTPUT
 LOC CYCLE SUCCESSFULLY COMPLETED
 WOULD YOU LIKE TO IMPLEMENT ANOTHER DESIGN (Y/N)?

Block Diagrams

Narrow Down The Search For The Right PLD

The programmable logic device market is constantly changing and improving. The *Programmable Logic Device Handbook* makes it easy for you to keep up with such rapidly advancing technology. With the *PLD Handbook*, you'll know what kinds of devices are available as well as their advantages and disadvantages from both a designer's and user's point of view. You'll choose the right type of device, and use it most effectively, to maximize circuit density and bring new levels of speed and logic power to your digital circuit designs.

About the Author

Von L. Burton, a 23-year veteran of the Marshall Space Flight Center, is responsible for the reduction of data generated by payloads that fly onboard the space shuttle. In addition he is an adjunct professor of statistics at Athens State College, Alabama, where he received an Outstanding Teaching Award in 1982.

Burton's work experience has involved such projects as: optimizing the flight trajectory of the Saturn V moon rocket; planning advanced space vehicles, satellites and payloads; performing mission operations analysis on payloads; and developing payload requirements for a space platform.

Recognized by NASA with two Outstanding Achievement Awards and a Sustained Superior Performance Award, Burton received a Space Concept Development Team Award for his initial conceptual creations in the origination of Spacelab and an IUS Failure Investigation and Anomaly Recovery Team Award.

Burton holds a B.A. in mathematics from Morehouse College, Atlanta, Georgia; an M.B.A. from Alabama A & M University, Huntsville; and a D.Sc. in computer sciences and systems, specializing in data communications from Southeastern Institute of Technology, Huntsville, Alabama.